REMARKS

The claims have been amended to recite that the insulation layer interposed between the SOI layer and the supporting substrate wafer of the bonded SOI substrate of the present invention comprises an insulation film formed on an entire surface of an active substrate forming the SOI layer and/or on an entire surface of the supporting substrate and that the plurality of cavities of the insulation layer have an opening area having a circular, elliptical, triangular, rectangular or other polygonal shape in a plan view of the insulation layer.

Support for the amendments to the claims is found in the specification disclosure of the present application on page 4, lines 1-3, and the description of the formation of the embodiments of the bonded SOI substrate of the present invention as illustrated in Figs. 1-9, in which an insulation film is formed on the entire exposed surface of an active layer wafer 10 (see page 13, lines 3-6) or supporting substrate wafer (see page 16, lines 7-9, and the paragraph bridging pages 18 and 19).

In the Action, claims 16 and 18-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruel, U.S. Patent No. 5,804,086; claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bruel in view of Hsu, U.S. Patent No. 6,114,197;

and claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Bruel.

Applicants respectfully submit that Bruel is insufficient to support a case of anticipation of claims 16 and 18-22 (as amended) under 35 U.S.C. § 102 and that the combination of Bruel and Hsu is insufficient to support a case of prima facie obviousness of claims 17 and 23-26 (as amended) under 35 U.S.C. § 103(a).

Referring, first, to the 35 U.S.C. § 102 rejection of the claims over Bruel, as shown in Fig. 2 of Bruel, multiple trenches 10 are formed in a network pattern in the surface of a silicon substrate (Fig. 2, Col. 4, lines 30 - 31), and a structure where a thin silicon film 16 is bonded to this surface is disclosed. In Bruel, the structure is one where the silicon film 16 for a surface for forming devices is bonded onto the silicon substrate and heat dissipation is improved by means of multiple trenches 10 provided in a network pattern extending to the edge (periphery) of the substrate. The maximum length for the trenches 10 is the same as the diameter of the wafer (Col. 4, lines 22 - 23).

Conversely, in the present invention, an oxide (insulation) film is formed on the entire surface of the silicon substrate in the present invention, and a silicon layer is formed with the interposition of this oxide film. Multiple cavities with different

heights are provided in the bonding surface. By this means, devices having different functions, such as CMOS logic and memory function cells, can be formed adjacent to each other in a single SOI layer. In addition, each cavity has a polygonal shape, e.g., circular shape, elliptical shape and the like, in a plane view and has a prescribed opening area (described in paragraphs [0014] and [0070] of the published application). In other words, each cavity is constituted as a sealed, or confined, space between the SOI layer and the silicon substrate. Therefore, the cavities in the present invention do not extend to the periphery of the wafer and are not open to the outside. Thus, the cavities recited in the claims of the present invention are not trenches extending from edge to edge on the wafer as in the structure of Bruel, and do not provide an improvement in the heat dissipation.

In addition, the trenches disclosed in Bruel all have the same depth because of the etching process (Fig. 3). This is because, as has been noted previously, these trenches are provided to improve heat dissipation capacity. On the other hand, closed cavities of differing depths are formed in various planes in the bonded SOI substrate of the present invention.

In the present invention, cavities with different depths are formed by techniques such as etching using multiple photomasks. An

insulating layer having cavities of different heights can be formed using these cavities. By varying the height of the cavities, the thickness of the insulating layer can be changed freely within a plane, and for example, the thickness of the insulating layer can be freely established.

Bruel discloses that the shape of the trenches can be changed. However, this means that the shape of all of the trenches is changed at the same time. There is no disclosure of multiple trenches differing in depth within a plane in Bruel. Moreover, there is no disclosure of making the depth of each trench different within a plane and being able to set the depth of the SOI layer freely.

Furthermore, an oxide film or other insulating film is formed over the entire surface in an active layer wafer or support substrate wafer in the present invention. By this means, the present invention can form an SOI layer with varied thicknesses over the entire surface of the wafer, and in addition, it is possible to form an insulating layer with varying thicknesses along with the cavities. In addition, since the present invention forms an insulating film over the entire surface of an SOI substrate, it can improve the insulating properties of the substrate more than the structure disclosed in Bruel.

Bruel does not form an insulating film on active layer wafers or support substrate wafers. Therefore, Bruel does not form an SOI layer in locations where no cavities are formed.

For the foregoing reasons, Bruel does not disclose, explicitly or inherently, each of the limitations of the rejected claims and is insufficient to support a case of anticipation of these claims under 35 U.S.C. § 102.

Hsu does not overcome the deficiencies of Bruel, is not logically or properly combinable with Bruel, and even if combined with Bruel, the bonded SOI substrate recited in the present claims will not result.

Hsu discloses a SIMOX SOI substrate provided with electrostatic protection. The invention described in Hsu is a method for forming an SOI substrate using a SIMOX method. A SIMOX method is one for forming an embedded oxide film by high temperature annealing after oxygen ions have been implanted in a silicon substrate using ion implantation. Such method is not a method for forming a bonded SOI substrate.

Since Hsu does not form a bonded SOI substrate, there is no disclosure of active layer wafers or support substrate wafers. Therefore, there is no suggestion of forming cavities by bonding active layer wafers and support substrate wafers.

In the present invention cavities of different depths are formed in the surface of an active layer wafer or a support substrate wafer. If this wafer then undergoes a thermal oxidation process, an oxide layer (insulating layer) can be formed at different depths from the surface over the entire surface of the wafer.

Conversely, since an oxide layer is formed using ion implantation in the invention described in Hsu, the continuous parts of the oxide layer with different depths must overlap in both areas when an oxide layer with different depths is formed. Therefore, there can be no optimal conditions for the oxygen dose amount, and there is a problem with crystal defects occurring in this part.

Furthermore, as noted above, in Bruel substrates are manufactured by bonding. On the other hand, in Hsu SOI substrates are manufactured by a SIMOX method. There is no suggestion in Bruel that the substrate manufacturing method using bonding can be applied to an SOI substrate manufacturing method using a SIMOX method. Similarly, there is no suggestion in Hsu that the SOI substrate manufacturing method using a SIMOX method can be applied to a substrate manufacturing method using bonding.

A person skilled in the art, therefore, is not provided with a proper motive for combining Bruel and Hsu as proposed in the Action.

Moreover, the heights of the cavities in the structure of Bruel are all the same, whereas in Hsu, the thickness of the SOI layer varies and, even if Bruel and Hsu are combined, an SOI layer of varying thickness will be layered on an oxide film formed in one plane, and the SOI substrate created will have steps in the surface of the SOI layer. Therefore, an SOI substrate having a single plane as in the present invention cannot be manufactured.

For the above reasons, the combination of Bruel and Hsu does not support a case of prima facie obviousness under 35 U.S.C. § 103(a) of the bonded SOI recited in the claims of the present application and removal of the 35 U.S.C. § 103(a) rejection is in order.

The foregoing is believed to be a complete and proper response to the Office Action dated January 27, 2006, and is believed to place this application in condition for allowance. If, however, minor issues remain that can be resolved by means of a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number indicated below.

In the event that this paper is not considered to be timely filed, applicants hereby petition for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 111833.

In the event any additional fees are required, please also charge our Deposit Account No. 111833.

Respectfully submitted,

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